Abstract

Two comparators are arranged to generate a pulse-width modulator (PWM) control pulse. The first comparator is arranged to start the PWM control pulse, while the second comparator is arranged to stop the PWM control pulse. The first comparator can be a high speed CMOS comparator that includes a built-in offset. The first and second comparators can be arranged such that the built-in offset of the first comparator dominates the overall operation at the start of the control pulse. The start of the PWM control pulse is initiated by a ramp voltage and a predetermined reference level instead of a clock edge. The PWM control pulse can be linearly varied down to a zero pulse width. The PWM control pulse may be used to control the on-time of the switching element in a switching-type converter.

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